



Timing Analysis and Simulation for Signal Integrity Engineers

Greg Edlund

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Every day, companies call upon their signal integrity engineers to make difficult decisions about design constraints and timing margins. *Can I move these wires closer together? How many holes can I drill in this net? How far apart can I place these chips?* Each design is unique: there's no single recipe that answers all the questions. Today's designs require ever greater precision, but design guides for specific digital interfaces are by nature conservative. Now, for the first time, there's a complete guide to timing analysis and simulation that will help you manage the tradeoffs between signal integrity, performance, and cost.

Writing from the perspective of a practicing SI engineer and team lead, Greg Edlund of IBM presents deep knowledge and quantitative techniques for making better decisions about digital interface design. Edlund shares his insights into how and why digital interfaces fail, revealing how fundamental sources of pathological effects can combine to create fault conditions. You won't just learn Edlund's expert techniques for avoiding failures: you'll learn how to develop the right approach for *your own* projects and environment.

Coverage includes

- Systematically ensure that interfaces will operate with positive timing margin over the product's lifetime—*without* incurring excess cost
- Understand essential chip-to-chip timing concepts in the context of signal integrity
- Collect the right information upfront, so you can analyze new designs more effectively
- Review the circuits that store information in CMOS state machines—and how they fail
- Learn how to time common-clock, source synchronous, and high-speed serial transfers
- Thoroughly understand how interconnect electrical characteristics affect timing: propagation delay, impedance profile, crosstalk, resonances, and frequency-dependent loss
- Model 3D discontinuities using electromagnetic field solvers
- Walk through four case studies: coupled differential vias, land grid array connector, DDR2 memory data transfer, and PCI Express channel
- Appendices present a refresher on SPICE modeling and a high-level conceptual framework for electromagnetic field behavior

Objective, realistic, and practical, this is the signal integrity resource engineers have been searching for.

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